REMARKS/ARGUMENTS

Entry of this Amendment as well as reconsideration and allowance of the subject application are respectfully requested.

Claim 1 now incorporates the subject matter of cancelled claim 8, as do independent claims 11 and 12. No new issues have been raised by incorporating this already examined feature of claim 8 in the independent claims, and therefore, the Amendment is proper and should be entered.

Accordingly, the rejection of claims 1, 11 and 12 under 35 USC §103 being unpatentable over Gulley in view of Messina should be withdrawn.

In view of this incorporation of the subject matter of claim 8 into the independent claims, the only relevant rejection to address is that under 35 USC §103 based on Gully in view of Messina and further in view of Langendorf et al. This rejection is respectfully traversed.

Gulley discloses a graphics floating point coprocessor 1200 designed to work in conjunction with a host graphic processor 120. The coprocessor 1200 performs arithmetic matrix calculations. Gulley lacks multiple features of the independent claims. First, the Examiner admits that Gulley fails to teach that the number of loaded data words loaded into the coprocessor 1200 depends on whether the start address of the operand data is aligned with a word boundary. As explained in the response to the previous Office Action, Gulley also fails to disclose that the coprocessor 1200 is:

> responsive to a coprocessor load instruction on said main processor to load one or more loaded data words into said coprocessor and perform at least one coprocessor processing operation specified by said coprocessor load instruction using said one or more loaded data words to provide operand data to generate at least one result data word.

In response to that distinction raised in the last response, the Examiner has replied in the remarks section on pages 10-11 of the Final Office Action:

> Gulley teaches that the coprocessor is responsive to a coprocessor load instruction (an instruction received from the host) on the main processor (the graphics processor in which the instruction comes from the host) to load one or more loaded data words (a set of operands) into the coprocessor and perform at least one coprocessor processing operation (the operation to be performed on the operands) specified by the coprocessor load instruction (the instruction received from the host) using the one or more loaded data words (the set of operands) to provide operand data to generate at least one result data word (the result) (e.g. see Col. 2, lines 3-10 and Fig.1).

However, the coprocessor of Gulley is not "responsive to a coprocessor load instruction on the main processor to load one or more loaded data words and perform at least one coprocessor processing operation specified by the coprocessor load instruction." In Gulley, the coprocessor accepts from the host "a set of operands and an instruction as to the operation to be performed." There is simply no teaching in Gulley that a load instruction used to load the operand data into the coprocessor also specifies the operation to be performed by the coprocessor on the loaded operand data. Neither Messina nor Langendorf disclose this feature. Accordingly, the independent claims patentably distinguish over the applied prior art.

There is another feature of the independent claims lacking from the applied prior art that forms a separate basis for finding claims 1, 11 and 12 patentable over the three applied references. The Examiner considers that Messina discloses the feature (which Gulley admittedly lacks) that "in response to said coprocessor load instruction a variable number of loaded data words are loaded into said coprocessor in dependence upon whether a start address of said operand data within said one or more loaded data words is aligned with a word boundary." Applicants disagree.

First, Messina does not relate to loading data words into a coprocessor. Messina does not even describe a coprocessor. Instead, Messina relates to the transfer of data between a main memory and a cache. Messina fails to disclose that the cache data transfer techniques can be applied to loading instructions into a coprocessor.

Second, even if one of ordinary skill in the art were to assume the techniques described in Messina could be applied to loading data into a coprocessor, (Applicants strongly disagree with such an assumption), Messina does not load a variable number of words into a cache. Although Messina reads a variable number of quad words (QWs) from a main memory, Messina writes (loads) a requested (not variable) number of double words (DWs) into the cache. The fixed number of requested DWs is extracted from the variable number of QWs. See column 4, line 45 to column 5, line 10. In Messina, only 8 QWs are stored into a line of the cache because this is the maximum number of QWs allowed in a cache line. If the requested DWs must be extracted from 9 QWs in the main memory due to a lack of alignment of the first requested DW with the QW boundary,

then only the second DW in the first QW is stored into the cache line. Similarly, only the first DW of the final QW is stored into the cache line. This is not a variable number. Accordingly, Messina, like Gulley, fails to disclose the feature that "a variable number of loaded data words are loaded into said coprocessor."

Further, there would have been no motivation to combine the teachings of Gulley and Messina. Messina does not load a variable number of data words into a coprocessor, but instead loads a fixed number of data words (double words) into a cache memory. Messina does not describe coprocessors. The Examiner's motivation to combine Gulley and Messina thus comes from the present application and therefore is improperly based on hindsight.

The independent claims recite that "said coprocessor includes an alignment register for storing a value specifying alignment between said operand data and said one or more loaded data words." The Examiner admits that neither Gulley nor Messina disclose this feature and relies on Langendorf. Langendorf relates to a branch cache system using a plurality of memory sets in which alignment bits are used to specify whether a corresponding branch target address terminates at the end of a parcel.

The system architecture described in Langendorf is completely different than that described in either Gulley or Messina. There is no relationship whatsoever between Langendorf and Gulley. The only relationship between Langendorf and Messina is that they both involve the alignment of one unit of data with another unit of data. But the particular data types involved are completely different, and the teachings of Langendorf

are irrelevant because an indication of alignment is already provided in Messina by the DW address bit 28. In other words, there would have been no motivation to combine Messina and Langendorf because Langendorf's teachings do not add to Messina's teachings in relevant respects.

Langendorf also fails to disclose a coprocessor. The alignment values of Langendorf are therefore not part of any coprocessor and are certainly not stored in an "alignment register" of a coprocessor. The alignment values in Langendorf do not specify alignment between operand data and loaded data words, but instead specify alignment between a branch instruction and a data parcel containing the end-point of the branch instruction. Accordingly, the alignment values do not serve as a trigger to specify a variable number of data words to be loaded into a coprocessor, as is the case in the independent claims that improve transfer efficiency.

Consequently, even with using three references in an attempt to find all of the features recited in the independent claims 1, 11 and 12, the Examiner has been unsuccessful. There are multiple features of the independent claims not disclosed or suggested by the applied patents. In addition to using three references, which by itself suggests a hindsight-based obviousness rejection, there is no proper motivation (for the reasons explained above) for combining the references of Gulley, Messina and Langendorf.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

CARPENTER et al
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Respectfully submitted,

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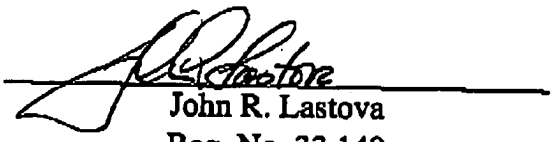
By: 
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